PECVD, ICP, E-beam or other suitable deposition method, over the etched layer of GaN **32** and between the gate **17** and the layer of p-type Al_yGaN **25**. The insulating layer **35** can further reduce gate leakage current increase gate turn on voltage and provide passivation. The insulating layer can be deposited either before or after forming the ohmic contacts for the source **18** and drain **19**. If the insulating layer **35** is deposited before the formation of the ohmic contacts, portions of the layer can be removed or left in place where metallization is to be deposited for the ohmic contacts. Both the device of FIG. **39** and FIG. **41** device do not require a regrowth step.

[0084] Referring to FIG. **42**, an N-face device is formed that has a selectively doped access region. The access region is doped by thermal diffusion of donor species from a dielectric (or other suitable) dopant diffusion layer **75** in the access region. The dopant diffusion layer **75** can include donor species, such as Si, SiO_2, SiN_x and other suitable donor species. The dopant diffusion layer **75** is annealed to cause the dopant (Si in case of Si, SiO_x or SiN_x) to migrate into the device and increase the 2DEG density in the access regions, thereby causing the device to have a lower on-resistance. The thermal diffusion can be carried out at any suitable temperature, for example between about 300 and 1000° C. To enhance the breakdown voltage of the device, multiple diffusions can be performed to mimic a lightly doped drain structure. In some embodiments, the dopant diffusion layer **75** is removed after annealing.

[0085] Referring to FIG. **43**, in an alternative embodiment to the device in FIG. **42**, instead of a dopant diffusion layer **75**, a dielectric layer which functions as a Fermi level pinning layer **78** is applied on the device. The pinning layer **78** can be either doped or undoped. The pinning layer **78** induces charge in the access region. Referring to FIG. **44**, in some embodiments the pinning layer is not only in the access region, but is also formed on the p-type Al_zGaN cap **11**. The cap **11** blocks any effects from the pinning layer **78** on the device in the gate region and thus the pinning can be on the cap without adversely causing a 2DEG in the gate region. The pinning layer **78** can be a layer of SiN_x, such as a layer of SiN_x grown by MOCVD, PECVD, CATCVD or other suitable means, including a combination of various deposition techniques. SiN_x on N-face or Ga-face III-nitride devices can pin the surface Fermi level close to the conduction band, resulting in high electron concentration and increased conductivity under the SiN_x region. The pinning layer **78** can be deposited at any suitable step in the fabrication sequence of the device, such as before the ohmic metal contacts are deposited or after. The pinning layer can be removed from the gate, source or drain contacts where electrical contact will be made.

[0086] FIGS. **45-48** show a variety of features that can be used with any of the devices described herein. Although the devices shown are N-face devices, the features can also be used with Ga-face devices.

[0087] Referring to FIG. **45**, a SiN_x cap **80** can be applied to the N-face of the cap during an early stage of processing and is selectively removed at a desired step in the process. N-face III-nitride devices can be more susceptible to damage than Ga-face III-nitride devices. Thus, the SiN_x cap **80** serves to protect the N-face surface from undesired damage during processing. The SiN_x cap **80** can be thin, such as less than 2000 Angstroms, for example, 100 Angstroms. In some embodiments, part of the SiN_x cap **80** is left in the gate region to function as a gate insulator.

[0088] Referring to FIG. **46**, in some embodiments, a dielectric passivation layer **83** is formed on an N-face device. The passivation layer **83** can be SiN_x or other suitable passivation material. The passivation material can be deposited by CVD, such as PECVD, MOCVD or ICP or by evaporation. In addition, an optional field plate **87** is formed over the gate region to reduce the peak electric field and help trapping and breakdown voltage capacity. The field plate **87** can be terminated at the source or at the gate.

[0089] Referring to FIG. **47**, a slant field plate **93** can be applied to an N-face device. The slant field plate **93** maximizes breakdown voltage. The slant field plate can be applied along with a dielectric passivation layer **83**. In some embodiments, such as the embodiment shown, the slant field plate **93** is integrated with the gate.

[0090] Referring to FIG. **48**, a device can be formed with a gate insulator **96** and/or an AlN inter-layer **97** between the GaN channel layer **41** and the Al_xGaN layer **43**. The gate insulator **96** is between the gate and the top semiconductor layer, such as the p-type cap or the channel layer. The gate insulator can minimize gate leakage. The gate insulator **96** is formed of a suitable insulating material, such as SiN_x, SiO_2 or AlN. The layer of AlN **97** between the GaN channel layer **41** and the Al_xGaN layer **43** is thin, such as greater than 0 to about 30 Angstroms. This layer improves the mobility-2DEG density product, resulting in a device with lower resistance.

[0091] Throughout the specification and in the claims, where III-nitride materials are described, a modification of the material may be used in its place so long as the material is not modified in such a way to reverse the intended polarization, e.g., by hindering the 2DEG in an access region or by inducing charge in the gate region. For example, where use of GaN is described, small amounts of aluminum or indium, e.g., up to 15%, 10%, 5% or 2% may be included in the GaN layer without deviating from the scope of the disclosed methods and devices. Similarly, where AlGaN materials are described, AlInGaN materials can be used in their place. That is, any of the GaN materials that are described can be replaced by secondary, tertiary, or quaternary materials, which are based on varying the amounts of the III type material of AlInGaN, Al, In and Ga, from 0 to 1, or $Al_xIn_yGa_{1-x-y}N$. When Al_xGaN material is described, $0<x<1$, $Al_xGa_{1-x}N$ can be substituted. Further, when a subscript for a group III material is used in the specification, such as x, y or z, a different letter may be used in the claims. Throughout the specification, ≧ or < may be substituted by ≧or ≦, respectively and ≧ or ≦ can be substituted by > or <, respectively.

[0092] Throughout the specification and in the claims, the Al_xGaN layer adjacent to the channel layer and responsible for forming a heterostructure with and 2DEG in the channel layer, can be doped at least in part. In embodiments, the doping is n-type. Throughout the specification, the GaN buffer layer is generally semi-insulating but in some embodiments may include a small portion, such as a portion furthest from the substrate side of the buffer layer, that is doped. This doping can be either n-type or p-type.

[0093] The devices described herein can be formed on a substrate of sapphire, silicon carbide (either Si-face or C-face), silicon, aluminum nitride, gallium nitride or zinc oxide. Although not shown in the various epilayer structure schematics, a transition layer or a nucleation layer can be formed on the substrate to facilitate the growth of the III-nitride layers. The nucleation layer is specific to the type of substrate used.